WE CLAIM:

1. An apparatus for receiving data from a distribution substation, wherein the distribution substation is configured to provide encoded data in a power signal on a distribution line in a power distribution network, the apparatus comprising:

a receiver conditioning block that is coupled to the distribution line, wherein the receiver conditioning block is positioned downstream from the distribution substation at an endpoint, and wherein the receiver conditioning block is arranged to provide an analog signal that is responsive to the power signal from the distribution line; and

a receiver processing block that is coupled to the receiver conditioning block, wherein the signal processing block is configured to extract the encoded data from the power signal by under-sampling the analog signal, and processing the under-sampled analog signal such that fundamental and harmonic frequencies associated with the power signal are suppressed.

2. The apparatus of claim 1, wherein the receiver conditioning block includes at least one of: a level control block, an anti-aliasing filter block, wherein the level control block is configured to provide attenuation to the power signal, wherein the anti-aliasing filter block is configured to pass signals in a defined frequency band.

3. The apparatus of claim 1, wherein the receiver processing block is further configured to process frequencies in the range from approximately 555Hz to 585Hz.

4. The apparatus of claim 3, wherein the data is encoded on the power signal as a frequency shift keyed (FSK) signal using inverted non-return-to-zero signaling (INRZ) at frequency tones correspond to approximately 555Hz and 585Hz.

5. The apparatus of claim 1 wherein: the power distribution network includes three conductors, where each conductor conducts a respective power signal having a

respective phase, and wherein the power signal corresponds to at least one of the respective power signals.

6. The apparatus of claim 1 wherein the receiver processing block is arranged to under-sample the analog signal at a rate that is locked to approximately ten times a frequency that is associated with the power signal.

7. The apparatus of claim 1 wherein the receiver processing block includes a first and second signal processing block, wherein the first signal processing block is arranged to provide a down-converted signal by sampling the analog signal at an under-sampled rate, and wherein the second signal processing block is arranged to re-sample the down-converted signal to provide a base-band signal, wherein the encoded data is extracted from the base-band.

8. The apparatus of claim 7, wherein the first signal processing block comprises:

an analog-to-digital converter block that is arranged to receive the analog signal and provide a sampled signal that is sampled at an under-sampled rate;

a power-line frequency rejection filter block that is arranged to receive the sampled signal and provide a first filtered signal such that fundamental and harmonic frequencies associated with the power signal is suppressed in the first filtered signal;

a low-pass filter block that is arranged to reject higher order frequencies from the first filtered signal;

an automatic gain control block that is arranged to provide a gained signal by adjusting a signal level that is associated with the first filtered signal; and

a second low pass filter block that is arranged to provide the down-converted signal in response to the gained signal by rejecting higher order frequencies from the gained signal.

9. The apparatus of claim 8, wherein the second signal processing block comprises:

a sampling block that is arranged to receive the down-converted signal and provide a re-sampled signal that is further down-converted;

a high pass filter block that is arranged to provide a second filtered signal in response to the re-sampled signal such that lower order frequencies associated with re-sampled signal are suppressed in the second filtered signal;

a quadrature detector block that is arranged to provide a base-band signal in response to the second filtered signal; and

a low pass filter block that is arranged to extract the encoded data in response to the base-band signal.

10. The apparatus of claim 1, further comprising a receiver frequency locked loop (FLL) that is arranged to provide a sampling clock for the receiver processing block by locking the sampling clock to a frequency that corresponds to approximately ten times the frequency associated with the power signal.

11. The apparatus of claim 10, further comprising an endpoint processor unit that is configured to provide the receiver frequency locked loop through a combination of hardware and software functions.

12. The apparatus of claim 10, further comprising an endpoint processor unit that is configured to provide the sampling clock for the receiver processing block by adjusting an interrupt time interval that is associated with the endpoint processor unit such that the interrupt time interval is locked to a rate that corresponds to approximately ten times the frequency that is associated with the power signal.

13. The apparatus of claim 12, wherein the endpoint processing block is further arranged to: capture a first timer signal when a zero-crossing is detected in the power

signal, capture a second timer signal when the tenth occurrence of the zero-crossing is detected by an interrupt, compute a difference between upper bytes of the first timer signal and the second timer signal, compare the difference to a last error signal, increase an error signal when the difference is greater than the last error signal, decrease the error signal when the difference is less than the last error signal, calculate a correction signal from the error signal using a proportional gain block and a differential gain block, gain the correction signal, and adjust a time interval associated with the interrupt in response to the gained correction signal.

14. An apparatus for generating a receiver clock frequency from a power signal, comprising:

a first capture block that is arranged to capture a first timer signal when a zero-crossing is detected in the power signal;

a second capture block that is arranged to capture a second timer signal when the tenth occurrence of the zero-crossing is detected by an interrupt;

a difference block that is arranged to provide a first difference signal that corresponds to a difference between upper bytes of the first timer signal and the second timer signal;

a comparator block that is responsive to the first difference signal and the last error signal;

a first summer block that is arranged to increase an error signal when the first difference signal is greater than the last error signal, and further arranged to decrease the error signal when the first difference signal is less than the last error signal;

a delay block that is arranged to provide the last error signal in response to the error signal;

a second summer block that is arranged to subtract the last error signal from the error signal to provide a second difference signal;

a first gain block that is arranged to provide a proportional signal in response to the error signal, where the proportional signal is related to the error signal according to a proportional gain factor;

a second gain block that is arranged to provide a differential signal in response to the second difference signal, where the differential signal is related to the second difference signal according to a differential gain factor;

a third summer block that is arranged to combine the proportional signal and the differential signal to provide a correction signal; and

a fourth summer block that is arranged to increase a timer adjustment signal in response to the correction signal such that a time interval associated with the interrupt is adjusted by changing the timer adjustment signal.

15. An endpoint that is arranged to communicate with a distribution substation with a power signal over a distribution line in a power distribution network, the endpoint comprising:

a means for receiving that is arranged to receive the power signal from the distribution line;

a means for sampling that is arranged to down-convert the received power signal to a base-band signal;

a means for locking that is arranged to lock a sampling rate that is associated with the means for sampling to a multiple of the frequency that is associated with the power signal; and

a means for extracting that is arranged to extract a digital bit stream from the base-band signal.

16. The endpoint of claim 15, further comprising: a means for detecting that is arranged to detect the receipt of a packet from the digital bit stream, a means for retrieving that is arranged to retrieve the packet, a means for evaluating that is arranged to evaluate

the retrieved packet, and a means for extracting that is arranged to extract commands from the retrieved packet when the packet does not contain errors.

17. The endpoint of claim 16, wherein the extracted commands comprise at least one of: assigning a transmit frequency, assigning a channel, assigning a sub-channel, defining a CRC, defining a packet format, synchronizing a date, synchronizing a time, updating a time-of-use map, adjusting a peak setting, selecting a transmission start time, selecting a time for recording electric meter readings, assigning an endpoint to a group, resetting the system, and starting a demand reporting interval.

18. The endpoint of claim 15, further comprising: a means for recording that is arranged to record metering data in the endpoint.

19. The endpoint of claim 15, further comprising:

a means for detecting that is arranged to detect a power-up condition;

a means for evaluating that is arranged to evaluate the power-up condition to determine a power-fault status; and

a means for updating that is arranged to update power-failure statistics when a power-fault is detected, wherein the power-fault status corresponds to at least one of: initial power-up, momentary interruption, momentary event, and sustained interruption.

20. The endpoint of claim 19, further comprising:

a means for triggering that is arranged to trigger unscheduled events in the endpoint; and

a means for processing that is arranged to process unscheduled events after the unscheduled event is triggered.

21. The endpoint of claim 19, further comprising:

a means for scheduling that is arranged to schedule events in the endpoint;

a means for triggering that is arranged to trigger scheduled events in the endpoint; and

a means for processing that is arranged to process scheduled events after the scheduled event is triggered.

22. The endpoint of claim 19, further comprising:

a means for selecting that is arranged to select a packet type based on the current day of the week;

a means for assembling that is arranged to assemble a packet for transmission based on the selected packet type; and

a means for starting that is arranged to start a packet transmission after the packet is assembled for transmission.